EAST SEARCH

11/21/03

L#	Hits	Search String	Databases
L2	2	5,465,216.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	2	5,513,122.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	2	5,859,962.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	2	5,901,073.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	2	5,913,022.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	2	5,905,883.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	2	5,937,183.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	2	5,966,516.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L12	2	5,974,575.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L13	4367	((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	375	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (function$1 \	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	18	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (function$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	15	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (function$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	4371	((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L6	28	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (circuit with t	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L8	40	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and ("state spac	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L7	16	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and ("state spac	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L9	27	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (reachable w	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L10	2	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (reachable \	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L11	2	(((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and ("state spa	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	0	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (consequen	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	7	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (consequent	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L1	0	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (reachable \	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	15	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (successive	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	4	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (reachable \	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	2	((((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and ("state spac	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
	48	(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (successive	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

09/630348 Yu-Chin Hsu

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Results of search set L10:(((digital or integrated) adj circuit) with (simulat$3 or verification or verify$3)) and (circuit with transition$1 with edge$1)

Document Kind Codes Title Issue Date Current OR Abstract

US 20030192014 A1	Simulator of dynamic circuit for silicon critical path debug	20031009	716/4
US 20030179025 A1	Delay lock loop having an edge detector and fixed delay	20030925	327/158
US 20030149924 A1	Method and apparatus for detecting faults on integrated circuits	20030807	714/726
US 20030128022 A1	Method of testing an integrated circuit by simulation	20030710	324/121E
US 20030036893 A1	Method and apparatus for simulating transparent latches	20030220	703/16
US 20020109535 A1	Power on reset circuit arrangement	20020815	327/143
US 20020036539 A1	Post-silicon methods for adjusting the rise/fall times of clock edges	20020328	327/566
US 20020035708 A1	Method and apparatus for generating test patterns used in testing semiconductor integrated c	20020321	714/25
US 20020011827 A1	Fault simulation method and fault simulator for semiconductor integrated circuit	20020131	324/71.5
US 20010037421 A1	Enhanced highly pipelined bus architecture	20011101	710/305
US 20010027549 A1	Method and apparatus for testing the timing of integrated circuits	20011004	714/734
US 6593765 B1	Testing apparatus and testing method for semiconductor integrated circuit	20030715	324/765
US 6532574 B1	Post-manufacture signal delay adjustment to solve noise-induced delay variations	20030311	716/6
US 6496953 B1	Calibration method and apparatus for correcting pulse width timing errors in integrated circuit	20021217	714/744
US 6493659 B1	Power consumption calculating apparatus and method of the same	20021210	703/14
US 6461882 B2	Fault simulation method and fault simulator for semiconductor integrated circuit	20021008	438/17
US 6407602 B1	Post-silicon methods for adjusting the rise/fall times of clock edges	20020618	327/170
US 6331800 B1	Post-silicon methods for adjusting the rise/fall times of clock edges	20011218	327/566
US 6289476 B1	Method and apparatus for testing the timing of integrated circuits	20010911	714/718
US 6148436 A	System and method for automatic generation of gate-level descriptions from table-based des	20001114	716/18
US 6059450 A	Edge transition detection circuitry for use with test mode operation of an integrated circuit mei	20000509	714/724
US 6009531 A	Transition analysis and circuit resynthesis method and device for digital circuit modeling	19991228	713/400
US 5959485 A	Controllable one-shot circuit and method for controlling operation of memory circuit using sam	19990928	327/227
US 5649176 A	Transition analysis and circuit resynthesis method and device for digital circuit modeling	19970715	713/400
US 5600787 A	Method and data processing system for verifying circuit test vectors	19970204	714/30
US 5486783 A	Method and apparatus for providing clock de-skewing on an integrated circuit board	19960123	327/147
US 4949341 A	Built-in self test method for application specific integrated circuit libraries	19900814	714/736
US 6059450 A	Test mode initializing and verification method for integrated circuit memory device, involves ir	20000509	